



(19)

Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 1 111 572 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
27.06.2001 Bulletin 2001/26

(51) Int Cl.7: **G09G 1/16**

(21) Application number: 00128013.0

(22) Date of filing: **20.12.2000**

(84) Designated Contracting States:
**AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE TR**
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 21.12.1999 JP 36234599

(71) Applicant: EIZO NANO CORPORATION
Ishikawa 924-8566 (JP)

(72) Inventors:

- **Nitta, Tatsuhisa, c/oEizo Nanao Corporation
Ishikawa 924-8566 (JP)**

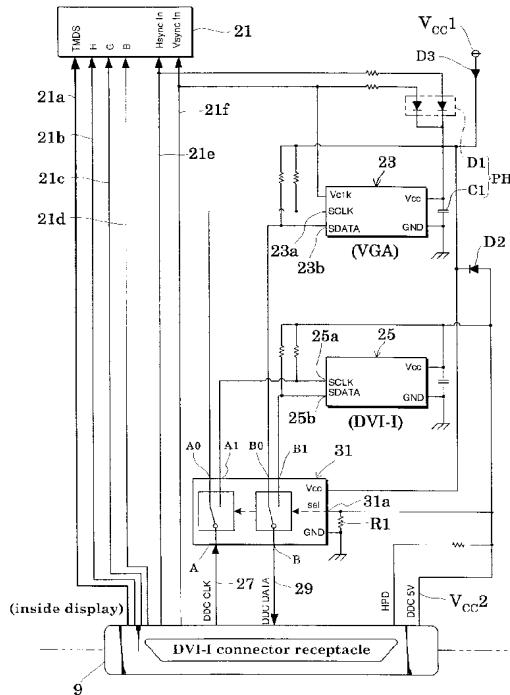
- Kawagoshi, Osamu, c/oEizo Nanao Corporation
Ishikawa 924-8566 (JP)
- Imamaki, Noritaka, c/oEizo Nanao Corporation
Ishikawa 924-8566 (JP)

(74) Representative:
Leson, Thomas Johannes Alois, Dipl.-Ing.
Tiedtke-Bühling-Kinne & Partner GbR,
TBK-Patent,
Bavariaring 4
80336 München (DE)

(54) **Display apparatus**

(57) A display apparatus for displaying images based on signals received from a host. The apparatus includes a determining means for determining an interface type of the host, a plurality of storage means each storing specification information relating to display for one of interface types to be connected, and an output means for outputting, from one of the storage means to the host, the specification information corresponding to the interface type determined by the determining means.

Fig.2



Description

BACKGROUND OF THE INVENTION

(1) Field of the Invention

[0001] This invention relates to a display apparatus connected to a host such as a graphics card in a computer for displaying images based on signals from the host.

(2) Description of the Related Art

[0002] Interface with a D-Sub connector, which is a typical type of analog interface, is chiefly used to connect a graphics card in a computer with a display apparatus.

[0003] The D-Sub connector is also called a 15-pin D-Shell display connector, a standard 15-pin VGA (Video Graphics Adapter) connector, or a VGA connector confirming to MIL-C-24308 Standard. In this specification, it will be called a VGA connector and the type of analog interface using this connector will be called a VGA interface. In this case, digital signals are converted to analog signals in the graphics card and the analog signals are transmitted to the display apparatus. The display apparatus processes the analog signals therein to display images.

[0004] Recently, it has become technically possible that display apparatus such as liquid crystal display apparatus accept digital signals as they are, and process and visualize these signals. Along with this trend, DVI-I, a digital interface using a new connector which is quite different from the VGA connector in shape, has been developed, and display apparatus having such interface are becoming commercially available.

[0005] DVI-I is the abbreviation of Digital Visual Interface Integrated which is the interface type that handles both TMDS (Transition Minimized Differential Signaling) digital signals and RGB (red, green and blue) analog signals.

[0006] A display apparatus having the DVI-I interface has a problem such that it cannot be physically connected to the graphics card having the VGA interface without a VGA/DVI-I conversion cable.

[0007] Even if the display apparatus is physically connected to the graphics card by using such a conversion cable, there is still another problem as mentioned hereinafter.

[0008] A computer operating system (hereinafter called an OS) today performs what is known as the Plug-and-Play function. Thus, when a Plug-and-Play compatible display apparatus is connected to a graphics card in a computer, the OS of the computer selects a driver (software) appropriate for display of images and automatically makes optimal settings for proper display.

[0009] To realize this function, the Plug-and-Play compatible display apparatus has specification informa-

tion already stored in its memory, which is to be transmitted to the graphics card. This specification information is called EDID (Extended Display Identification Data), and includes, for example, the resolution, frequency of vertical scan signals, frame rate, vendor code indicating the manufacturer's name, and the serial number of the display apparatus. Naturally, this information varies with models of display apparatus. Even display apparatus of the same model may have different information according to the interface type employed by the display apparatus.

[0010] Consequently, even when a graphics card having the VGA interface and a display apparatus having the DVI-I interface are connected through the conversion cable, EDID may not be transmitted normally to the graphics card. Even when EDID is transmitted, the Plug-and-Play function may not be performed normally. Then, no images will be displayed on the screen of the display apparatus, or appropriate display will not be achieved according to the specification of the display apparatus.

SUMMARY OF THE INVENTION

[0011] This invention has been made having regard to the state of the art noted above, and its object is to provide a display apparatus for selectively outputting appropriate specification information corresponding to the interface type on the host side to display images properly according to the specifications.

[0012] The above object is fulfilled, according to this invention, by a display apparatus for displaying images based on signals received from a host, comprising a determining means for determining an interface type of the host, a plurality of storage means each storing specification information relating to display for one of interface types to be connected, and an output means for outputting, from one of the storage means to the host, the specification information corresponding to the interface type determined by the determining means.

[0013] Signals from the host such as a graphics card in a computer reflect the interface type of the host. The determining means can determine the interface type from these signals. Alternatively, the user may manually operate a selector switch or the like, whereby the determining means may determine the interface type based on the state of the switch. The output means outputs specification information corresponding to the interface type determined, from one of the storage means to the host. Consequently, the host can make optimal settings for proper display according to the specification information.

[0014] Thus, according to this invention, the display apparatus can display images properly according to its specification even when the interface type of the host is different from that of the display apparatus.

[0015] Preferably, the determining means is arranged to discriminate between the latest DVI-I interface and the conventional VGA interface.

[0016] In this case, the output means outputs appropriate specification information corresponding to the interface type, whichever is employed by the host, so that images can be displayed properly according to the specification of the display apparatus.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] For the purpose of illustrating the invention, there are shown in the drawings several forms which are presently preferred, it being understood, however, that the invention is not limited to the precise arrangement and instrumentalities shown.

[0018] Fig. 1 is an overall view of a computer system including a display apparatus according to this invention;

[0019] Fig. 2 is a block diagram of a principal portion of the display apparatus; and

[0020] Fig. 3 is a view showing a conversion cable.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] Preferred embodiments of the present invention will be described in detail hereinafter with reference to the drawings.

[0022] Referring to Fig. 1, a computer 1 has a keyboard 3 and a mouse 5 connected thereto for inputting instructions and the like. The computer 1 outputs images and other data to a display 8 through a graphics card 7 inserted into an extended slot of the computer 1. The display 8 has a receptacle 9 formed adjacent to the rear thereof for receiving a DVI-I connector for the DVI-I interface.

[0023] The graphics card 7 corresponds to the host of this invention. This graphics card 7 may be the VGA interface type, or the DVI-I interface type.

[0024] Where the interface type is different, signals from the graphics card 7 and a voltage to a DC power line are different. Specification information called EDID is also different, which is outputted from the display 8 to the graphics card 7 to allow proper display of images on the display 8. The EDID acts on the OS of computer 1 most effectively where the OS supports the Plug-and-Play function.

[0025] Where, for example, the graphics card 7 employs the VGA interface and the display 8 employs the DVI-I interface, the graphics card 7 and display 8 must be connected through a conversion cable 13 having, at both ends thereof, a VGA connector acting as a receptacle 10 and a DVI-I connector acting as a plug 11. The DVI-I connector 11 has a 5V line for DDC (Display Data Channel) which is grounded as described hereinafter.

[0026] Where both the graphics card 7 and the display 8 employ the DVI-I interface, the graphics card 7 and display 8 may be connected through a usual video cable, i.e. one for the DVI-I interface.

[0027] The display 8 includes a display screen such

as a liquid crystal display screen, and an ASIC 21 for controlling this display screen (Fig. 2). The ASIC 21 has a TMDS signal line 21a which is a digital signal line, RGB signal lines 21b-21d, a horizontal synchronizing signal line 21e and a vertical synchronizing signal line 21f, all extending from the DVI-I connector receptacle 9 to the ASIC 21. Through this ASIC 21 signals are exchanged between various components (not shown) of the display

8.

[0028] The display 8 includes two EDID storage memories 23 and 25 which correspond to the storage means of this invention. The EDID storage memory 23 is for the VGA interface and the EDID storage memory 25 is for the DVI-I interface. These memories 23 and 25 store

EDID corresponding to the respective interfaces. Synchronously with a clock from a DDC clock line 27 received at serial clock terminals 23a and 25a, the memories 23 and 25 output the EDID from serial data terminals 23b and 25b to a DDC data line 29.

[0029] The storage means are not limited to the two EDID storage memories 23 and 25. The number of memories may be varied with the number of interface types to be accommodated. Each memory may be selected for each interface type by a multiplexer 31.

[0030] The serial clock terminals 23a and 25a of EDID storage memories 23 and 25 are connected to input terminals A0 and A1 of multiplexer 31. The serial data terminals 23b and 25b are connected to input terminals B0 and B1 of multiplexer 31. Output terminals A and B of multiplexer 31 are selectively connected to the input terminal A0 or A1 and the input terminal B0 or B1, respectively, according to a voltage at a selector terminal 31a. In this embodiment, when the voltage at the selector terminal 31a is "0V" or thereabout, the output terminals A and B are connected to the input terminals A0 and B0, respectively. When the voltage is "5V" or thereabout, the output terminals A and B are connected to the input terminals A1 and B1, respectively.

[0031] The multiplexer 31 corresponds to the determining means and output means of this invention.

[0032] A power line Vcc1, which is connected to the primary source of display 8 for supplying 5V DC voltage, is connected to the EDID storage memory 23 and to the multiplexer 31 through a backflow preventing diode D3 which prevents reverse flow of current. Power is constantly supplied to the EDID storage memory 23 and multiplexer 31 during the operation of the display 8, including the operation in a power save mode. The horizontal synchronizing signal line 21e and vertical synchronizing signal line 21f are connected to the power terminal of EDID storage memory 23 through a rectifier diode D1. The rectifier diode D1 forms a peak hold circuit PH in combination with a capacitor C1 connected between the power terminal and a grounding terminal.

[0033] A power line Vcc2 (5V line for DDC) is connected to the power terminal of EDID storage memory 23 through a rectifier diode D2. The rectifier diode D2 forms a peak hold circuit PH in combination with a capacitor C2 connected between the power terminal and a grounding terminal. That is, when the power line Vcc1 is at "0V", power needed for the operation is obtained from the graphics card 7.

[0034] A power line Vcc3 (5V line for DDC) is connected to the power terminal of EDID storage memory 25 through a rectifier diode D3. The rectifier diode D3 forms a peak hold circuit PH in combination with a capacitor C3 connected between the power terminal and a grounding terminal.

ed to the selector terminal 31a of multiplexer 31, and is grounded through a resistor R1. Consequently, even when the power line Vcc2 is opened instead of being grounded, the selector terminal 31a is forcibly reduced to "0V" unless a voltage is applied.

[0034] Further, the power line Vcc2 is connected directly to the power terminal of EDID storage memory 25, and through a DC backflow preventing diode D2 to the power terminal of EDID storage memory 23. This backflow preventing diode D2 prevents a current from the peak hold circuit PH from flowing into the power line Vcc2. The backflow preventing diode D2 also prevents the current from flowing to the selector terminal 31a of multiplexer 31 in order not to reverse the operation of multiplexer 31.

[0035] Referring to Fig. 3, the conversion cable 13 extends between the DVI-I connector 11 and the VGA connector 10. The DVI-I connector 11 has a power line Vcc3 (5V line for DDC) which is grounded.

[0036] For the reason noted hereinbefore, this power line Vcc3 may be opened instead of being grounded.

[0037] The RGB signal lines 21b-21d, horizontal synchronizing signal line 21e, vertical synchronizing signal line 21f, DDC clock line 27 and DDC data line 29 are connected to the corresponding terminals of the DVI-I connector 11 and the VGA connector 10.

[0038] Operation of the apparatus having the above construction will be described next.

<DVI-I connector>

[0039] Where the graphics card 7 has a connector of the DVI-I interface, the graphics card 7 and display 8 are connected through a digital video cable (not shown) having DVI-I connectors at both ends thereof.

[0040] In this case, 5V voltage for DDC is supplied to the power line Vcc2 to supply power to the multiplexer 31 and is also supplied to both EDID storage memory 23 and EDID storage memory 25, thereby activating the two memories 23 and 25. The 5V voltage is applied to the selector terminal 31a of multiplexer 31.

[0041] Consequently, the input terminals A1 and B1 of multiplexer 31 are selected and only the operative state of the EDID storage memory 25 is transmitted to the graphics card 7 even though both EDID storage memories 23 and 25 are activated.

<When power to the display is off>

[0042] When power supply to the display 8 is completely cut off, the power line Vcc1 becomes "0V". However, power is supplied from the power line Vcc2 to the EDID storage memory 25 and to the multiplexer 31. Consequently, even though the display 8 is turned off, the EDID is normally transmitted to the graphics card 7 to perform the Plug-and-Play function normally.

<VGA connector>

[0043] Where the graphics card 7 has a connector of the VGA interface, the graphics card 7 and display 8 are connected through the conversion cable 13.

[0044] The display 8 supplies power to the power line Vcc1 to activate the EDID storage memory 23 and the multiplexer 31. Since the power line Vcc2 is grounded, the selector terminal 31a of multiplexer 31 becomes "0V", whereby it selects the input terminals A0 and B0. Consequently, the EDID is outputted from the EDID storage memory 23.

[0045] Since no power is supplied to the EDID storage memory 25 which is unnecessary in this case, a relatively small power capacity generated in the peak hold circuit PH will not be wasted.

<When power to the display is off>

[0046] When power supply to the display 8 is completely cut off, except in the power save mode for reducing power consumption by the display 8, the power line Vcc1 becomes "0V".

[0047] However, the peak hold circuit PH supplies power to the EDID storage memory 23 and to the multiplexer 31.

[0048] Consequently, even though the display 8 is turned off, the EDID is normally transmitted to the graphics card 7 to allow proper display of images.

[0049] This invention is not limited to the construction in the foregoing embodiment, but may be modified as follows:

35 (1) In place of the above conversion cable, a simple VGA/DVI-I conversion cable not having, at its DVI-I end, any DDC 5V line which is opened or grounded may be used. In this case, the inputs to the multiplexer may be switched by manually operating a switch disposed at the rear of the display.

40 The DVI-I connector may have a projection or the like formed thereon. When this projection enters a recess formed at the rear of the display, a selector switch therein may be operated automatically to switch the inputs to the multiplexer.

45 (2) The storage means may be a single physical memory having an internal storage region logically divided to store EDID corresponding to a plurality of interface types. In this case, for example, the interface type may be determined by a microcomputer, and the EDID corresponding to the interface type may be retrieved from the memory and outputted in response to a serial clock detected by the microcomputer.

50 (3) The interface type is not limited to the described combination of the VGA interface and the DVI-I interface. The same advantages may be secured for other interface types by devising a way of distinguishing one type from another.

[0050] The present invention may be embodied in other specific forms without departing from the spirit or essential attributes thereof and, accordingly, reference should be made to the appended claims, rather than to the foregoing specification, as indicating the scope of the invention.

[0051] A display apparatus for displaying images based on signals received from a host. The apparatus includes a determining means for determining an interface type of the host, a plurality of storage means each storing specification information relating to display for one of interface types to be connected, and an output means for outputting, from one of the storage means to the host, the specification information corresponding to the interface type determined by the determining means.

Claims

1. A display apparatus for displaying images based on signals received from a host, comprising:

determining means for determining an interface type of said host;
a plurality of storage means each storing specification information relating to display for one of interface types to be connected; and
output means for outputting, from said storage means to said host, the specification information corresponding to the interface type determined by said determining means.

2. A display apparatus as defined in claim 1, wherein said determining means is arranged to determine the interface type based on a voltage value of a particular DC power line among signal lines from said host.

3. A display apparatus as defined in claim 2, wherein said output means comprises a multiplexer for selectively switching the connection to one of said plurality of storage means in response to said voltage value of said DC power line.

4. A display apparatus as defined in claim 1, wherein said determining means is arranged to discriminate between the DVI-I (Digital Visual Interface Integrated) interface and the VGA (Video Graphics Adapter) interface.

5. A display apparatus as defined in claim 1, wherein said plurality of storage means comprise two storage means, one for the DVI-I interface, and the other for the VGA interface, said storage means for the DVI-I interface being powered by said host only when the interface type is the DVI-I interface.

5. A display apparatus as defined in claim 5, further comprising a peak hold circuit for generating a DC voltage based on synchronizing signals received from said host, said DC voltage generated by said peak hold circuit being supplied only to said storage means for the VGA interface and to said multiplexer.

10. A display apparatus as defined in claim 6, further comprising a backflow preventing diode disposed between said peak hold circuit and said storage means for the DVI-I interface for blocking a DC current flowing from said peak hold circuit.

15. A display apparatus as defined in claim 4, wherein said display apparatus is connected to said host through a VGA to DVI-I conversion cable having, at its DVI-I end, a 5V line for DDC (Display Data Channel) which is opened or grounded.

20. A display apparatus as defined in claim 1, wherein said specification information is EDID (Extended Display Identification Data) necessary for the Plug-and-Play function.

25. 10. A display apparatus as defined in claim 2, wherein said specification information is EDID necessary for the Plug-and-Play function.

30

35

40

45

50

55

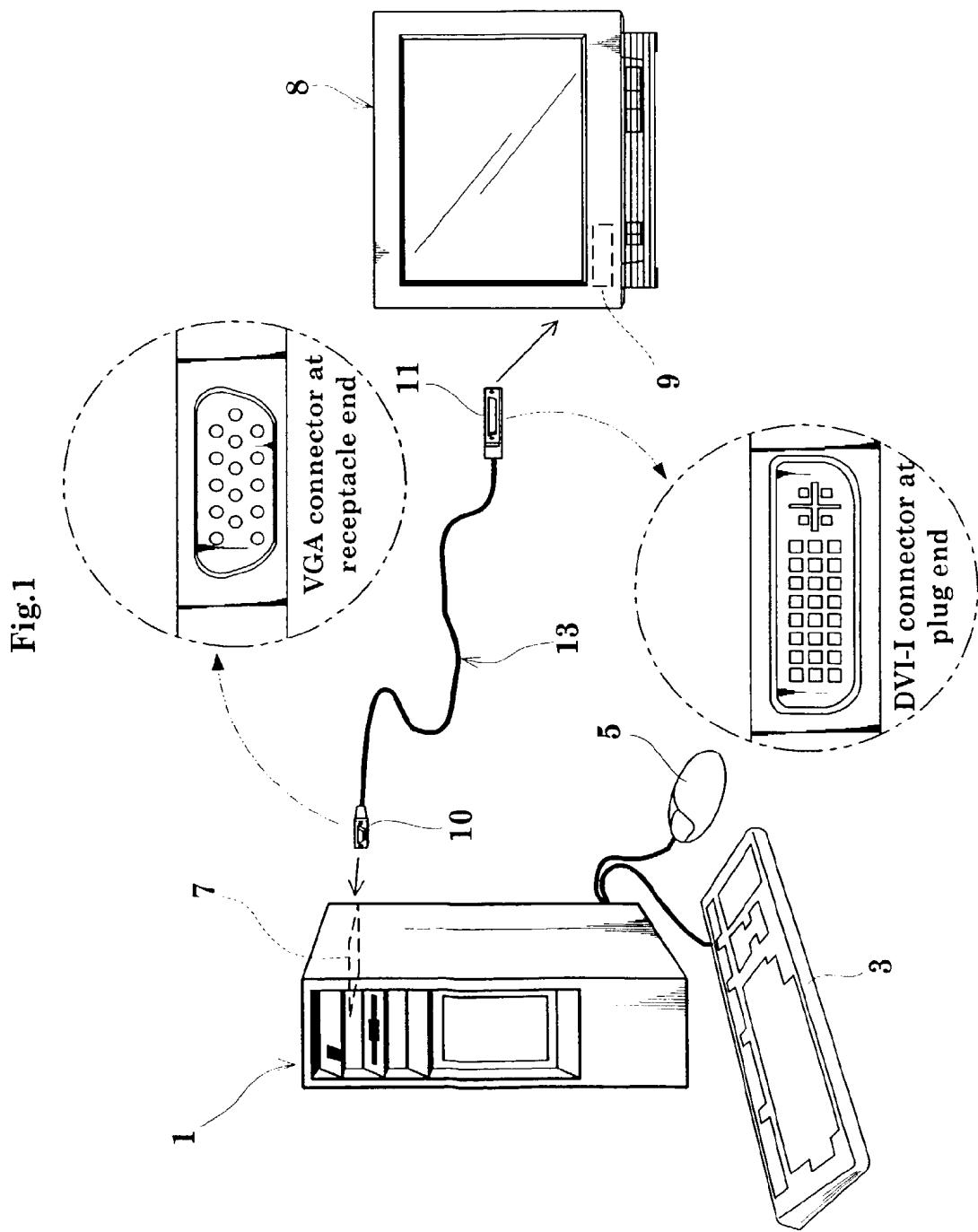


Fig.2

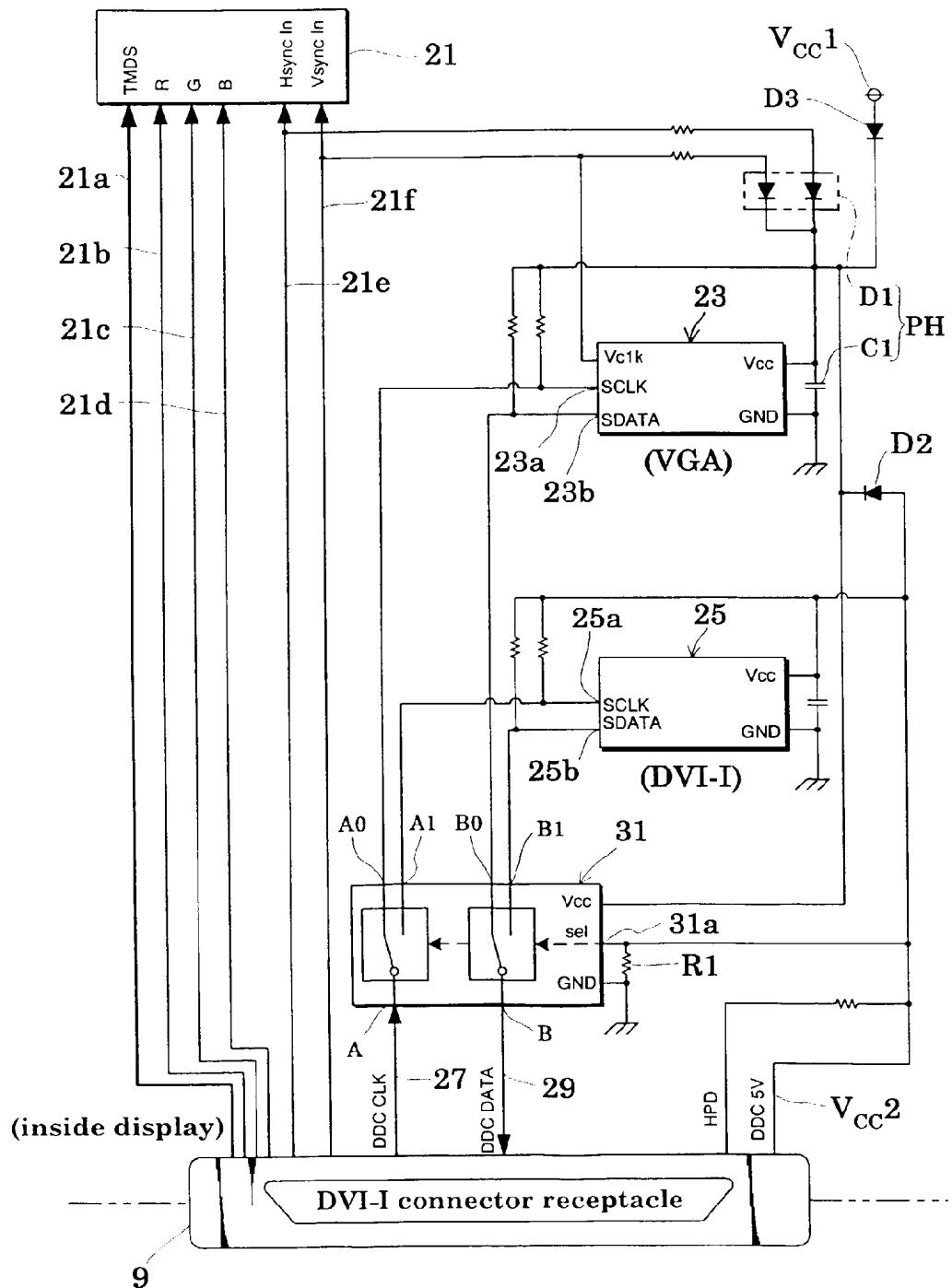
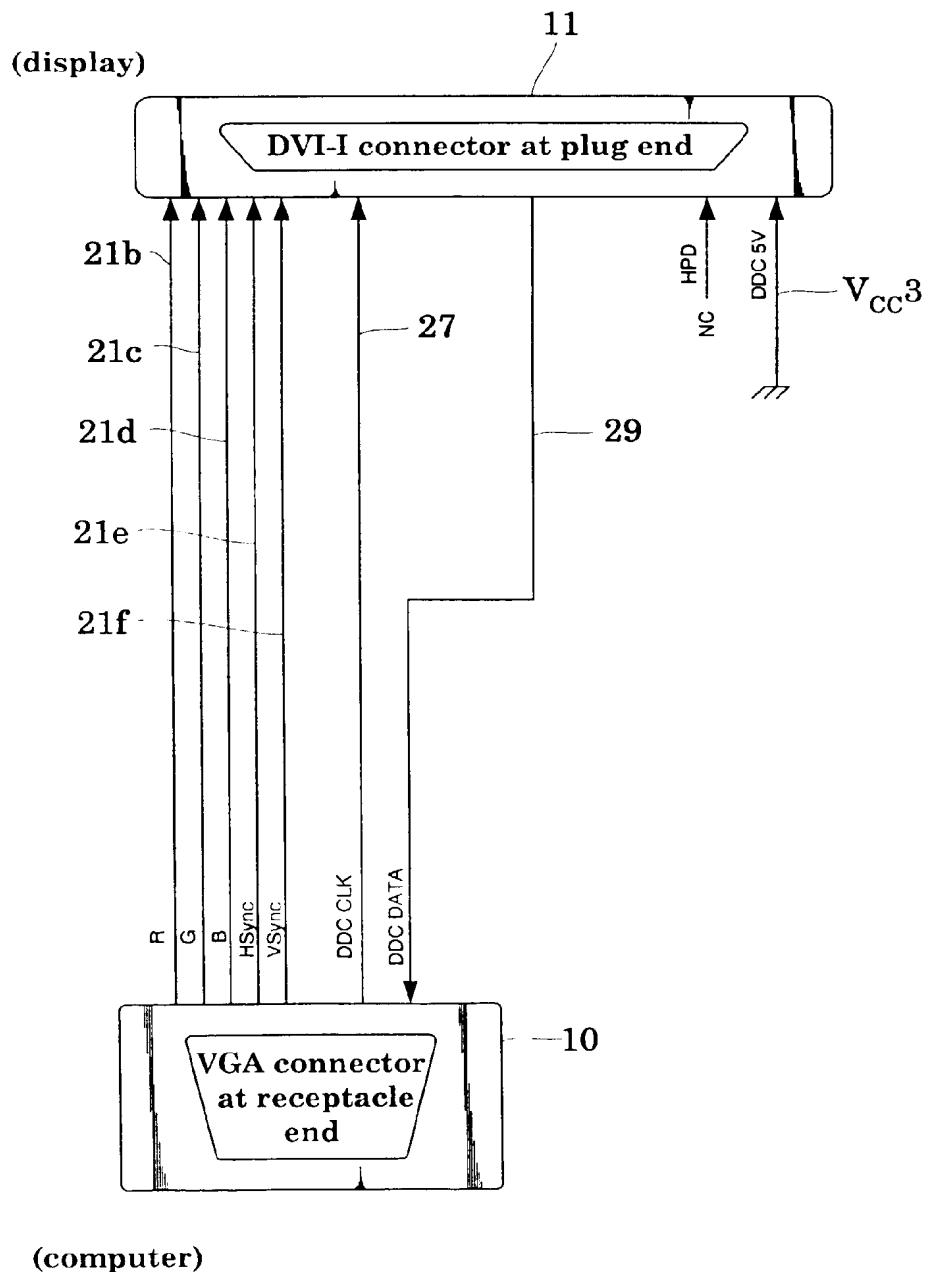


Fig.3



(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11)

EP 1 111 572 A3

(12)

EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
26.06.2002 Bulletin 2002/26

(51) Int Cl.7: G09G 1/16, G09G 5/00

(43) Date of publication A2:
27.06.2001 Bulletin 2001/26

(21) Application number: 00128013.0

(22) Date of filing: 20.12.2000

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 21.12.1999 JP 36234599

(71) Applicant: EIZO NANAO CORPORATION
Ishikawa 924-8566 (JP)

(72) Inventors:
• Nitta, Tatsuhisa, c/oEizo Nanao Corporation
Ishikawa 924-8566 (JP)

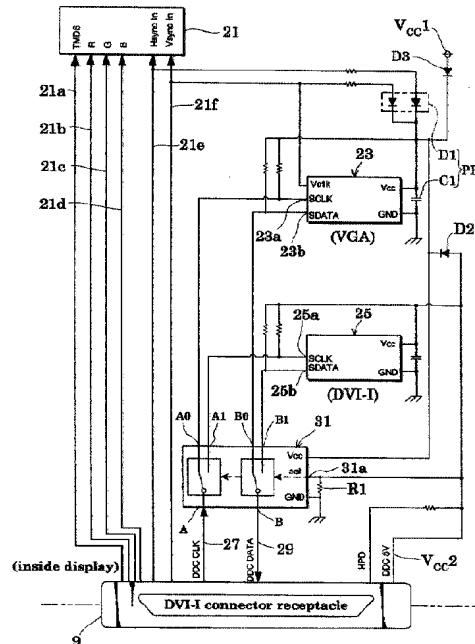
• Kawagoshi, Osamu, c/oEizo Nanao Corporation
Ishikawa 924-8566 (JP)
• Imamaki, Noritaka, c/oEizo Nanao Corporation
Ishikawa 924-8566 (JP)

(74) Representative:
Leson, Thomas Johannes Alois, Dipl.-Ing.
Tiedtke-Bühling-Kinne & Partner GbR,
TBK-Patent,
Bavariaring 4
80336 München (DE)

(54) Display apparatus

(57) A display apparatus for displaying images based on signals received from a host. The apparatus includes a determining means for determining an interface type of the host, a plurality of storage means each storing specification information relating to display for one of interface types to be connected, and an output means for outputting, from one of the storage means to the host, the specification information corresponding to the interface type determined by the determining means.

Fig.2





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 12 8013

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 13, 30 November 1999 (1999-11-30) -& JP 11 231994 A (TOSHIBA CORP), 27 August 1999 (1999-08-27) * abstract; figure 3 * * paragraphs [0002],[0006],[0015],[0018] *	1-3,9,10	G09G1/16 G09G5/00
Y	---	4,5	
Y	"DIGITAL VISUAL INTERFACE DVI" PAPER DIGITAL DISPLAY WORKING GROUP, XX, XX, 2 April 1999 (1999-04-02), pages 1-76, XP002948299	4,5	
A	* page 14, paragraph 2.2.5 *	8-10	
A	US 5 764 547 A (BILICH JAMES A ET AL) 9 June 1998 (1998-06-09) * column 4, line 66 - column 5, line 15; figure 2 *	6,7	

			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
			G09G
The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	3 May 2002	Amian, D	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone			
Y : particularly relevant if combined with another document of the same category			
A : technological background			
O : non-written disclosure			
P : intermediate document			

ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.

EP 00 12 8013

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

03-05-2002

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
JP 11231994	A	27-08-1999	NONE	
US 5764547	A	09-06-1998	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82